08/217,211, filed March 24, 1994, now abandoned; which is a continuation of Serial No. 07/811,063, filed December 20, 1991, now abandoned, and this application is a continuation-in-part of Serial No. 08/293,201 filed August 19, 1994 (now U.S. Patent 5,614,732); which was a continuation of Serial No. 07/967,564, filed October 28, 1992, now abandoned; which was a continuation of Serial No. 07/673,821, filed March 22, 1991, now abandoned.--

A1 cont'd

IN THE CLAIMS:

Please cancel claims 1-20.

Please add the following new claims:

Sub B1

A2

--21. An active matrix display device having a pixel portion and a peripheral circuit portion, said peripheral portion including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region; and

a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said thin film transistors in both of the pixel portion and a part of the peripheral circuit portion,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 cm^2 /V.sec or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 cm^2 /V. sec or more,

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^5$ to $1x10^{18}$ cm^{-3},

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

22. A semiconductor circuit having a pixel portion and a shift register, said shift register including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor. each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions ~~and a~~ channel region;

a gate insulating film adjacent to at least said channel region; and a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said thin film transistors in both of the pixel portion and the shift register,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 cm^2/V.sec or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 cm^2/V.sec or more,

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}cm^{-3}$,

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

23. A semiconductor circuit having a pixel portion and an inverter said inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region; and

a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said thin film transistors in both of the pixel portion and the inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V.sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V.sec$ or more,

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1s10^{15}$ to $1x10^{18}$ cm^{-3},

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

24. A semiconductor circuit having a pixel portion and a clocked inverter said clocked inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region; and a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said thin film transistors in both of the pixel portion and the clocked inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V.sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V.sec$ or more,

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^5$ to $1x10^{18}$,

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

25. An active matrix display device having a pixel portion and a peripheral circuit portion, said peripheral portion including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region; and a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said thin film transistors in both of the pixel portion and a part of the peripheral circuit portion,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V.sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V.sec$ or more, and

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3} to control an absolute value of a threshold voltage of said n-channel thin film transistor to be substantially the same as an absolute value of a threshold voltage of said p-channel thin film transistor,

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

26. A semiconductor circuit having a pixel portion and a shift register said shift register including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor

island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region; and a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said thin film transistors in both of the pixel portion and in the shift register,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V.sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V.sec$ or more, and

wherein at least one of ~~said semiconductor~~ semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3} to control an absolute value of a threshold voltage of said n-channel thin film transistor to be substantially the same as an absolute value of a threshold voltage of said p-channel thin film transistor,

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

27. A semiconductor circuit having a pixel portion and an inverter said inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region; and

a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said thin film transistors in both of the pixel portion and the inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V.sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V.sec$ or more, and

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3} to control an absolute value of a threshold voltage of said n-channel thin film transistor to be substantially same the as an absolute value of a threshold voltage of said p-channel thin film transistor,

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

28. A semiconductor circuit having a pixel portion and a clocked inverter said clocked inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region; and

a gate electrode adjacent to said gate insulating film,

a leveling film covering each of said thin film transistors in both of the pixel portion and the clocked inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V.sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V.sec$ or more, and

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of 1×10^{15} to $1x10^{18}$ cm^{-3} to control an absolute value of a threshold voltage of said n-channel thin film transistor to be substantially the same as an absolute value of a threshold voltage of said p-channel thin film transistor,

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less.

29. An active matrix display device having a pixel portion and a peripheral circuit

portion, said peripheral portion including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region; and

a gate electrode adjacent to said gate insulating film;

a leveling film covering each of said p-channel and n-channel thin film transistors in both of the pixel portion and a part of the peripheral circuit portion,

wherein said semiconductor ~~island~~ of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V.sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V.sec$ or more,

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3},

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less,

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7x10^{19}$ cm^{-3}.

30. A semiconductor circuit having a pixel portion and a shift register said shift register including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region; and

a gate electrode adjacent to said gate insulating film,

a leveling film covering each of said thin film transistors in both of the pixel

portion and the shift register,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V.sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V.sec$ or more,

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3},

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less,

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7x10^{19}$ cm^{-3}.

31. A semiconductor circuit having a pixel portion and an inverter said inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region; and

a gate electrode adjacent to said gate insulating film,

a leveling film covering each of said thin film transistors in both of the pixel portion and the inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V.sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V.sec$ or more,

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3},

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less,

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7x10^{19}$ cm^{-3}.

32. A semiconductor circuit having a pixel portion and a clocked inverter said clocked inverter including at least one pair of complementary p-channel and n-channel thin film transistors, and said pixel portion including at least one thin film transistor, each of said transistors comprising:

a crystalline semiconductor island on an insulating surface, said semiconductor island having source and drain regions and a channel region;

a gate insulating film adjacent to at least said channel region; and

a gate electrode adjacent to said gate insulating film,

a leveling film covering each of said thin film transistors in both of the pixel portion and the clocked inverter,

wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 10 $cm^2/V.sec$ or more and said semiconductor island of n-channel thin film transistor has an electron mobility in the range of 15 $cm^2/V.sec$ or more,

wherein at least one of said semiconductor islands comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3},

wherein each of said semiconductor islands has a thickness in the range of 5000 Å or less,

wherein each of said semiconductor islands comprises oxygen at a concentration not higher than $7x10^{19}$ cm^{-3}.

Sub D

33. A circuit according to any one of claims 22-24, 26-28, and 30-32 wherein said semiconductor is silicon.

34. A circuit according to any one of claims 22-24, 26-28, and 30-32 wherein said gate electrode comprises crystalline silicon doped with phosphorus.

35. A circuit according to any one of claims 22-24, 26-28, and 30-32 wherein said gate electrode is a multilayer film of crystalline silicon doped with phosphorus and a metal film thereon, said metal comprising at least a material selected from the group consisting of Mo, W, $MoSi_2$, and WSi_2.

36. A circuit according to any one of claims 22-24, 26-28, and 30-32 wherein said semiconductor island comprises oxygen at a concentration not higher than $1x10^{19}$ cm^{-3}.

37. A circuit according to any one of claims 22-24, 26-28, and 30-32 wherein said crystalline semiconductor island exhibits a Raman peak shifted to a lower frequency side from 522 cm^{-1}.

38. A circuit according to claim 34 wherein said phosphorus doped in said crystalline silicon is at a concentration of $1x10^{21}$ to $5x10^{21}$ cm^{-3}.

39. A circuit according to any one of claims 22-24, 26-28, and 30-32 wherein said source and drain regions of n-channel thin film transistor are introduced with phosphorus at a dose of $1x10^{15}$ to $5x10^{15}$ cm^{-3}.

40. A circuit according to any one of claims 22-24, 26-28, and 30-32 wherein said semiconductor island has a thickness of 500-5000 Å.

sub B7

41. An active matrix display device including a pixel portion and a peripheral circuit portion comprising:

a plurality of pixel electrodes formed on an insulating surface;

a first plurality of thin film transistors being formed in the pixel portion on said insulating surface and being connected to said pixel electrodes;

a second plurality of thin film transistors being formed in the peripheral circuit portion on said insulating surface, said second plurality of thin film transistors including at least one pair of complementary p-channel and n-channel thin film transistors;

a leveling film covering both of the first and second plurality of thin film transistors in the pixel portion and a part of the peripheral circuit portion,

wherein said second plurality of thin film transistors in said peripheral circuit include channel semiconductor layers having at least one of an electron mobility 15 $cm^2/V.s$ or more and a hole mobility of 10 $cm^2/V.s$ or more,

wherein each of the channel semiconductor layers comprises boron at a concentration in the range of $1x10^{15}$ to $1x10^{18}$ cm^{-3},

wherein each of said channel semiconductor layers has a thickness of 5000 Å or less.

42. An active matrix display device including a pixel portion and a peripheral circuit portion comprising:

a plurality of pixel electrodes formed on an insulating surface;

a first plurality of thin film transistors being formed in the pixel portion on said insulating surface and being connected to said pixel electrodes;

a second plurality of thin film transistors being formed in the peripheral portion on said insulating surface, said second plurality of thin film transistors including at least one pair of complementary p-channel and n-channel thin film transistors;

a leveling film covering both of the first and second plurality of thin film transistors in the pixel portion and a part of the peripheral circuit portion,

wherein said second thin film transistors in said peripheral circuit include channel semiconductor layers comprising silicon in which oxygen is contained at a concentration not higher than $7x10^{19}$ cm^{-3},

wherein each of said channel semiconductor layers has a thickness of 5000 Å or less.

~~43. A device according to claim 41 or 42 wherein said semiconductor is silicon.~~

~~44. A device according to claim 41 or 42 wherein each of the first and second plurality of said thin film transistors comprises a gate electrode formed over said channel semiconductor layers having a gate insulating film therebetween.~~

45. A device according to claim 44 wherein said gate electrode comprises crystalline silicon doped with phosphorus.

46. A device according to claim 44 wherein said gate electrode is a multilayer film of crystalline silicon doped with phosphorus and a metal film thereon, said metal comprising at least a material selected from the group consisting of Mo, W, $MoSi_2$, and WSi_2.

47. A device according to claim 45 or 46 wherein said phosphorus doped in said crystalline silicon is at a concentration of $1x10^{21}$ to $5x10^{21}$ cm^{-3}.

Sub B3

~~48. A device according to claim 41 or 42 wherein said channel semiconductor layers exhibit a Raman peak shifted to a lower frequency side from 522 cm^{-1}.~~

Cxm 49. A device according to any one of claims 21, 25, and 29 wherein said semiconductor is silicon.

50. A device according to any one of claims 21, 25, and 29 wherein said gate electrode comprises crystalline silicon doped with phosphorus.

51. A device according to any one of claims 21, 25, and 29 wherein said gate electrode is a multilayer film of crystalline silicon doped with phosphorus and a metal film

thereon, said metal comprising at least a material selected from the group consisting of Mo, W, $MoSi_2$, and WSi_2.

52. A device according to any one of claims 21, 25, and 29 wherein said semiconductor island comprises oxygen at a concentration not higher than 1×10^{19} cm^{-3}.

~~53. A device according to any one of claims 21, 25, and 29 wherein said crystalline semiconductor island exhibits a Raman peak shifted to a lower frequency side from 522 cm^{-1}.~~

54. A device according to claim 30 or 31 wherein said phosphorus doped in said crystalline silicon is at a concentration of 1×10^{21} to 5×10^{21} cm^{-3}.

~~55. A device according to any one of claims 21, 25, and 29 wherein said source and drain regions of n-channel thin film transistor are introduced with phosphorus at a dose of 1×10^5 to 5×10^5 cm^{-3}.~~

56. A device according to any one of claims 21, 25, and 29 wherein said semiconductor island has a thickness of 500-5000 Å.

~~57. A circuit according to any one of claims 22-24, 26-28, and 30-32, wherein said leveling film comprises an organic resin.~~

~~58. A circuit according to claim 57, wherein said organic resin is a transparent polyimide resin.~~

~~59. A device according to any one of claims 21, 25, 29, 41 and 42, wherein said leveling film comprises an organic resin.~~

60. A device according to claim 59, wherein said organic resin is a transparent polyimide resin.

sub B6

~~61. A circuit according to any one of claims 22-24, 26-28, and 30-32, wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 200 $cm^2/V.sec$ or less and said semiconductor island of n-channel thin film transistor has a electron mobility in the range of 300 $cm^2/V.sec$ or less.~~

~~62. A device according to any one of claims 21, 25, and 29, wherein said semiconductor island of p-channel thin film transistor has a hole mobility in the range of 200 $cm^2/V.sec$ or less and said semiconductor island of n-channel thin film transistor has a electron mobility in the range of 300 $cm^2/V.sec$ or less.~~

sub B7

~~63. A device according to claim 41, wherein said second plurality of thin film transistors in said peripheral circuit include channel semiconductor layers having at least one of an electron mobility 300 $cm^2/V.s$ or less and a hole mobility of 200 $cm^2/V.s$ or less.~~

sub D7

64. A circuit according to any one of the claims 22-24, and 30-32, wherein said n-channel thin film transistor has an approximately same absolute value of a threshold voltage as said p-channel thin film transistor.

65. A device according to any one of the claims 21, 25, 29, wherein said n-channel thin film transistor has an approximately same absolute value of a threshold voltage as said p-channel thin film transistor.

sub D8

66. A circuit according to claim 35 wherein said phosphorus doped in said crystalline silicon is at a concentration of $1x10^{21}$ to $5x10^{21}$ cm^{-3}.--